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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,594	05/16/2001	Toyohiko Yoshida	57454-116	9350

7590 07/20/2006

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,594	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-10 and 19* is/are pending in the application.

4a) Of the above claim(s) *3 and 11-18* is/are withdrawn from consideration.

5)☒ Claim(s) *10 and 19* is/are allowed.

6)☒ Claim(s) *1,2 and 4-9* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/16/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1,2,4-10,19 rare presented for examination. Claims 3 , 11-18 have been canceled.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,2,4,5,7,8,9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okado (EP 051 1484 A2) in view of Hennessy (Computer Architecture) in view of Dean (5,544,342).

4. Okado (EP 051 1484 A2) and Hennessy (Computer Architecture) were already cited to applicant on the record, therfore no copies are provided in this action.

5. As to claims 1 , 9, Okado taught a data processing system comprising at least :

a) an instruction memory in which an instruction is stored (see figure 1 , (201)), Column 9, lines 4-8 show that this ROM is a program or instruction memory.

b) a data memory in which data is stored (fig. 1 , element 101).,

c) an instruction decoder decoding a fetched instruction (fig.1 I D E C) ;

d) a memory operation unit (figure 1, elements 103 and 207) connected to the instruction memory, said data memory and said instruction decoder, fetching an instruction stored in said instruction memory, and accessing said data memory according to a decode result of said instruction decoder; (Col. 10, lines 12-15 show that

the repeat controller portion allows instructions to be read (fetched) from the micro ROM (instruction memory). Okado's Figure 1 showed a pointer portion is used to access the data memory based on the decoder output on line 202.) and an integer operation unit carrying out an integer operation based on a result of an instruction decoder, Figure 1 shows ALU 1 , which performs arithmetic functions and is an integer unit. The outputs 204 of the decoder. Column 9, lines 28-31 showed that this output of the decoder controls the arithmetic logic operations.)

5. As to the feature of memeory operation unit reads out data from data memory in claim 9, Okado also included a memory operation unit that reads out data from the data memory via a data input bus, and writes data into said data memory via a data output bus differing from said data input bus. Okado disclosed a bus that inputs data to the data memory and a separate bus that outputs data from the data memory (e.g. see fig.1)

6. Okado did not disclose the instruction memory including a plurality of instruction memory banks, and the memory operation unit generating a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out pipeline processing when a plurality of instructions are fetched from a plurality of said instruction memory banks. However, Hennessy disclosed the use of memory banks for memory systems (e.g. see in pages 361-363) . Page 362 shows that one memory bank initiation or read is completed per clock cycle. It showed that when

reading from multiple banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from. This selection must take place before fetching can occur and is inherently during a clock cycle. This cycle may be the same cycle as the transfer is made from the selected bank or it may be in a prior cycle, however in any case a pipeline cycle is generated that corresponds to the selection of the memory bank.

7. In addition, Hennessy shows that multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank (see Page 361). The faster speed of memory transfers would have motivated one of ordinary skill in the art to use multiple memory banks (as taught by Hennessy) in the instruction memory. It would have been obvious to one of ordinary skill in the art at the time of invention to use Hennessy into Okado with modified configuration parameters (e.g. the R/W port) to include a plurality of memory banks in the instruction memory system of Okado in order to increase the throughputs of the transfer operation of the memory, and therefore, provided a motivation.

Okado did not specifically show the memory operating unit for generating the pipeline cycle corresponding to the instruction readout to carry out the pipeline process as claimed. However, Dean disclosed a memory operation unit (see dynamic pipeline cycle generating unit in fig.15) for generating pipeline cycles corresponding to the instruction readout from a high speed memory (see instruction cache for high speed instruction memory in fig,15, see also col.25, lines 10-59). It would have been obvious to one of ordinary skill in the art to use Dean in Okado for including the memory

operation unit for generating pipelining cycle as claimed because the use of Dean could provide Okado the ability to process the instruction from the high speed memory (e.g. the cache) at reduced instruction cycles, such as the fetch and decode, in a predetermined pipeline sequence, and because Okado did teach a repeat controller portion which allowed instructions to be read (fetched) from the micro ROM (instruction memory, see Col. 10, lines 12-15), which was a suggestion of the need for memory operating unit for generating the pipeline cycle in order to minimize the latency of the instruction fetch in the ROM, and for doing so, provided a motivation.

8. Okado did not teach the memory operation unit generates a pipeline cycle corresponding to selection of an instruction memory bank and a pipeline cycle corresponding to instruction readout from said selected instruction memory bank to carry out pipeline processing when a plurality of instructions are fetched from a plurality of said instruction memory banks. Okado disclosed one memory bank initiation or read is completed per clock cycle (Page 362). However, Dean disclosed a memory operation unit (see dynamic pipeline cycle generating unit in fig.15) for generating pipeline cycles corresponding to the instruction readout from a high speed memory (see instruction cache for high speed instruction memory in fig,15, see also col.25, lines 10-59). The reasons of obviousness were already given in the paragraph above, therefore it will not be repeated herein.

9. As to claim 2, Okado did not explicitly show the first bank select circuit decoding an address including a low order address to generate chip select signals of the plurality of instruction memory banks so that a different instruction memory bank of the plurality of instruction memory banks is accessed when instructions at continuous addresses are accessed. However, It is most likely that if two instructions are stored at two memory addresses separated by the border of memory banks, that the memory bank must be switched to access the second instruction and that the low order address would play a role in chip-selecting the bank since it gives the border address of the

.

10. As to claim 4, Okado did not specifically disclose the accessing said plurality of data memory banks. However, Hennessy disclosed the use data memory when of memory banks for memory system (e.g. see pages 361-363). It shows that one memory bank initiation or read is completed per clock cycle , and that when reading from multiple banks, one bank is read from while the other is then selected in a generated cycle so that in the next generated cycle that bank is read from (Page 362) . Hennessy also showed multiple memory banks allow for producing or accepting one word fetched or stored per clock cycle, which is faster than using one memory bank (Page 361) . The faster memory transfers would have motivated one of ordinary skill in the art to modify Okado to use multiple memory banks in the data memory.
It would have been obvious to one of ordinary skill in the art at the time of invention to use Okado with Hennessy to include a plurality of memory banks in the data memory system as taught by Hennessy so that transfers of the memory

could be enhanced.

11. As to claim 5, Okado did not explicitly show the data memory further includes a second bank select circuit decoding an address including a high order address to generate chip select signals of said plurality of data memory banks in order to divide said plurality of data memory banks into two different regions. However, the examiner holds that it is most likely that a higher order address will divide a memory bank into two sections. The highest bit of a memory address that switches within a memory bank indicates two section of that memory bank.

12. As to claim 7, Okado did not disclose wherein said data memory generates a pipeline cycle corresponding to data access to carry out a pipeline process when accessing said high speed data memory. However, Hennessy disclosed caches in the memory hierarchy (pages 18-20). The cache did not have memory banks and therefore did not require a cycle to select a bank. A cache is a fast or high-speed memory. Hennessy showed that a cache is a fast or high-speed Local memory for holding commonly used information. The ability to have a fast memory to retrieve data from would have motivated one of ordinary skill in the ad to use Okado in view of Hennessy as applied above to include a data cache. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Okado in view of Hennessy as applied to above to include a cache as taught by Hennessy for storing instructions so that data could be retrieved faster.

13. As o claim 8, Okado in view of Hennessy disclosed a memory operation unit

fetches an instruction from said instruction memory via an instruction bus (Okado, figure 1 , 201 to IR1) and accesses said data memory via a data bus (figure 1 , Page 9 (106)) differing from said instruction bus.

14. Claims 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the second bank select circuit decodes the address including the low order address to generate the chip select of the memory banks so diffident memory bank is accessed when data at the continuous addresses in the two different regions are accessed.

15. Claims 10,19 are allowable over the art of record for reciting the combined details of the instruction memory, data memory, instruction decoder, the register file, the memory operating unit, he integer unit, the retaining of the loop instructions, the generation of the pipeline cycles, the first flag indicating a first execution at the first execution cycle and retaining the fetched instruction in the register file when repeat instruction was executed, the second flag indicating second execution cycle to the last execution cycle at the second execution cycle to the last execution cycle and executed the loop while fetching the instruction retained in the dedicated register.

18. Clam10 has been found physical transformation (see the memory operation unit coupled to instruction memory) and practical; application (see the low power consumption of the pipeline).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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